

**REMARKS**

The Office examined claims 1-14 and rejected same. With this paper, claims 1-4, 6-9 and 11-14 are amended, none are added and claims 5 and 10 are canceled.

**Claim Rejections under 35 USC §103**

Claims 1 and 3-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Valentaten et al (U.S. Patent 5,250,940, Valentaten hereinafter) in view of Niimura et al (U.S. Publication 2002/0154130 A1, Niimura hereinafter).

In the rejected claims, claims 1, 8 and 12 are independent.

With this paper, claim 1 is amended to recite an apparatus that comprises a memory and an adapter circuit. The apparatus connects a display device and a processor. Further, claim 1 specifies:

wherein the apparatus is configured to realize signaling between the processor and the display device connection interface, and

wherein the adapter circuit is configured to match signals between the memory bus and the display device connection interface by synchronizing the signals of the memory bus in an order required by the display device.

In the Office Action, the adapter circuit of the instant claim is asserted as being equivalent to the RAM arbiter 18 of Valentaten (page 2, section 3 of the Detailed Action). However, it is respectfully submitted that the function of the adapter circuit is different from that of the RAM arbiter.

According to the present invention, the adapter circuit 1) realizes signaling between the processor and the display device connection interface, and 2) matches signals between the memory bus and the display device connection interface by synchronizing the signals of the memory bus in an order required by the display device.

Valentaten teaches that the RAM arbiter 18 monitors the address references issued by the embedded processor 14 to identify when the embedded processor 14 seeks access to the RAM 12. Whenever there is no conflict with the embedded processor 14, the video function 16 uses the RAM bus for its own purpose (col. 4, lines 23-29). Valentaten further explains that: "The embedded processor 14 can execute instruction fetch cycles to the ROM 20 while the RAM bus is in use by the video function 16. This allows the embedded processor 14 to keep its instruction queue filled without interfering with the mover and video fetch machine. As stated above, the RAM arbiter 18 can identify the appropriate RAM bus cycles within which to execute video function access to RAM." (Col. 4, lines 30-37)

Thus, the function of the RAM arbiter 18 is, as indicated by its name, to regulate the signal traffic between the embedded processor 14 and the RAM 18. RAM 18 is a memory unit that is similar to the memory 305 of the instant invention. However, memory 305 is not a critical element in claim 1. It is clear from the above-quoted descriptions of Valentaten that the RAM arbiter does not serve to regulate signal traffic between the processor 14 and the video interface 16. Further, Valentaten does not disclose that signals are synchronized by the RAM arbiter in an order required by the video display.

Therefore, the combined teachings of Valentaten and Niimura do not include all the limitations of claim 1. Particularly, the limitation of claim 1, "wherein the adapter circuit is configured to match signals between the memory bus and the display device connection interface by synchronizing the signals of the memory bus in an order required by the display device" is neither disclosed by Valentaten nor by Niimura.

Based on the foregoing, claim 1 is patentable. Applicant respectfully requests the rejection of claim 1 and all dependent claims thereof be reconsidered and withdrawn.

Other independent claims are amended to be consistent with claim 1 and they include the same patentable features of claim 1. Therefore, these claims, and all dependent claims thereof, are patentable as well. Applicant respectfully requests the rejection under 35 USC §103(a) be reconsidered and withdrawn.

**Claim Rejections under 35 USC §112**

Claim 2 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office rejects claim 2 because it recites the matter that is represented by a trademark and which adds uncertainty.

Applicant respectfully submits that in a Preliminary Amendment submitted at the filing of the application, the trademark "Nokia Oyj" has already been removed. With this paper, claim 2 is further amended. Withdrawal of the rejection is respectfully requested.

**Conclusion**

It is believed that the application is now in condition for allowance, and early passage to issue is earnestly solicited. The Examiner is invited to contact applicant's agent at the number below if there are any questions.

Dated: 8/12/2008

Respectfully submitted,



Shiming Wu  
Agent for Applicant  
Reg. No. 56,885

WARE, FRESSOLA, VAN DER SLUYS  
& ADOLPHSON LLP  
Bradford Green, Building Five  
755 Main Street, P.O. Box 224  
Monroe, CT 06468  
Telephone: (203) 261-1234  
Facsimile: (203) 261-5676  
USPTO Customer No. 004955